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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 23/02 — A1

(11) International Publication Number: WO 95/15007

(43) International Publication Date: 1 June 1995 (01.06.95)

(21) International Application Number: PCT/US94/12460

(22) International Filing Date: 31 October 1994 (31.10.94)

(30) Priority Data:
08/162,750 29 November 1993 (29.11.93) US

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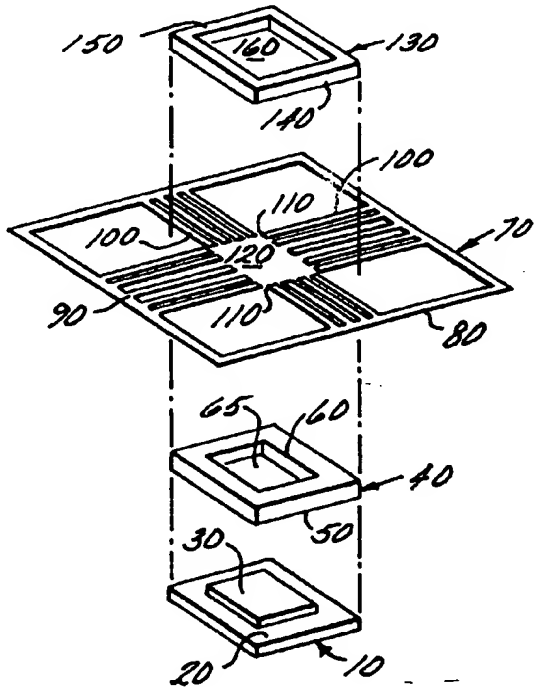
(81) Designated States: JP, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: ELECTRONIC CHIP CARRIER PACKAGE AND METHOD OF MAKING THEREOF

(57) Abstract

A method and design for packaging electronic chip devices, especially devices intended for radio frequency (RF) and microwave frequencies above 900 MHz is disclosed. An array of metal leads (100) are bonded between two layers of a sheet polymer composite that have been cut to form frames (40, 130) in such a way that the metal leads (100) extend from outside to inside of the single frame shape formed by a pressure and heat bonding step. The polymer composite frame serves the dual purpose of holding the leads in a desired configuration for later assembly and testing steps both inside and outside of its area, and of providing a microwave quality, low insertion loss, low permittivity and electrical insulation function between leads and ground planes. This dual purpose is provided in a uniquely cost-effective way that makes it of particular value for packaging high frequency electronic components intended for the growing consumer and commercial applications market.



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ELECTRONIC CHIP CARRIER PACKAGE AND METHOD OF MAKING THEREOF

Background of the Invention:

Field of the Invention

The invention relates to an improved chip carrier package and method of making the same such that the carrier is suitable for high radio frequency and microwave applications while maintaining low loss, low permittivity and low cost. The present invention finds particular utility in those applications requiring frequencies above 900 MHz.

Discussion of the Prior Art

The chip carrier industry has been aware for some time of the need for and design constraints of an alternative to high permittivity ceramic chip packages or molded plastic packages for packaging high frequency digital and analog chip devices for the growing requirements in commercial and consumer applications.

Ceramic packages with leads are produced cost-effectively by thick or thin film metallization of a ceramic layer which is then cofired with a cover piece of ceramic green sheet to form the frame with leads. Typically, the ceramics have

relatively high permittivity and the metal leads formed from firing powdered metal with glass frits have relatively high losses at high frequencies.

Molded plastic packages incorporating punched metal leads carried in a lead frame design have been used for many years for low cost packaging of digital electronic devices for the well known dual-in-line package (DIP). These packages normally use injection moldable thermoset composites to result in a package that will survive assembly operations such as soldering. While the leads in these packages can be low loss, the electrical loss of the dielectric at high frequencies limits their usefulness in microwave applications. In addition, such packages do not incorporate a conductive ground plane close to the die.

Chip devices or dies designed for high speed or high frequency applications are usually built on gallium arsenide (GaAs) substrates typically only about 100 micrometers thick. To realize planned performance at or above 900 MHz, the mounting surface must be a conductive ground plane. GaAs dies are typically mounted to the floor of a costly metal housing with gold-tin or gold-silicon solder. The cost of such packages is, therefore, unacceptably high. Moreover, there is no convenient way to pretest the die before the package is committed to it so there is a risk of a relatively high failure rate when commercially produced.

Summary of the Invention:

The above-discussed and other problems and deficiencies of the prior art are overcome or alleviated by the novel chip carrier package and method of manufacture thereof of the present invention. The present invention is intended for, and effective in overcoming deficiencies of, prior art chip carriers with respect to high frequency and microwave applications. Moreover, the method of constructing the chip carrier package of this invention is extremely cost effective and so, is economically desirable.

In accordance with the present invention, the chip carrier is constructed by providing a metallic base plate appropriately dimensioned and shaped to accept and

interconnect with a first layer frame of dielectric material having a low permittivity. Generally, the base plate will have a raised central portion which can be of any desired shape; the first frame layer of dielectric material then being shaped to fit over the raised portion in a cooperating manner. A lead frame, having been previously manufactured, and having an outer perimeter and finger-like leads extending inwardly therefrom, is placed upon the first frame layer of dielectric material so that the inner ends of the leads overlay the dielectric material.

It should be noted at this point that a line connecting the inner ends of the leads would define a space having a shape, preferably square or rectangular, similar to the shape of the raised portion of the base plate.

Once the lead frame is placed in position, a second frame layer of dielectric material is placed so as to sandwich the ends of the leads between the first and second frame layers of dielectric material. The second frame layer of dielectric material is shaped substantially similarly to the first frame layer and defines a void having the same shape as the space defined by the inner ends of the leads but having slightly larger dimensions, preferably square or rectangular.

After the base, first dielectric frame layer, lead frame and second dielectric frame layer are properly assembled, the entire structure is clamped and then heated to a temperature sufficient to soften the dielectric and thereby embed the leads in the dielectric material. This step is followed by a speedy cooling step to prevent the dielectric material from deforming in the areas not contacted by leads.

The chip carrier can subsequently be cut free from the lead frame by any of a number of conventional methods, such as punching. Leads are then available for desired bending and/or mounting.

It will be appreciated that other types of mounting arrangements for carriers, for example, plated through hole pins, etc. and many different configurations of chip carriers can be produced using the method of the invention.

As is clear from the foregoing, the resultant electronic chip carrier package comprises an array of metal leads bonded between two layers of a sheet polymer composite (e.g., filled fluoropolymer dielectric) that have been precut to form frames in such a way that the metal leads extend from outside to inside of the single frame shape formed by a pressure and heat bonding step. The polymer composite frame serves the dual purpose of holding the leads in a desired configuration for later assembly and testing steps both inside and outside of its area, and of providing a microwave quality, low insertion loss, low permittivity and electrical insulation function between leads and ground planes. This dual purpose is provided in a uniquely cost-effective way that makes it of particular value for packaging high frequency (e.g., greater than 900 MHz) electronic components intended for growing consumer and commercial applications market.

The above-discussed and other features and advantages of the present invention will be appreciated and understood by those skilled in the art from the following detailed description and drawings.

Brief Description of the Drawings:

Referring now to the drawings wherein like elements are numbered alike in the several FIGURES:

FIGURE 1 is an exploded, perspective view of the chip carrier of the invention;

FIGURE 2 is a top plan view of the assembled chip carrier with the lead frame still attached;

FIGURE 2a is a cross-section of FIGURE 2 taken along section line a-a.;

FIGURE 2b is a cross-section of FIGURE 2 taken along section line b-b;

FIGURE 3 is a perspective view of the completed chip carrier package of the invention;

FIGURE 4 is a top plan view of another embodiment of the invention showing five RF leads with widened sections outside of the package and 3 DC leads;

FIGURE 5 is a top plan view of another embodiment featuring a small space between the metallic base and the first dielectric layer;

FIGURE 5a is a cross-sectional view of FIGURE 5 taken along section lines a-a;

FIGURE 6 is a top plan view of a further embodiment; and

FIGURE 6a is a sectional view of FIGURE 6 taken along section lines a-a;.

FIGURE 6b is an enlarged side view of FIGURE 6 taken along section lines a-a.

FIGURE 7 is a perspective view of a dual in-line type of chip carrier package made by the invention.

FIGURE 7a is a side view of FIGURE 7.

FIGURE 7b is an end view of FIGURE 7.

FIGURE 7c is a top plan view of FIGURE 7.

FIGURE 8 is a perspective view of another embodiment of the invention where the entire carrier is enclosed in covering material.

FIGURE 8a is a side view of FIGURE 8.

FIGURE 8b is an end view of FIGURE 8.

FIGURE 8c is a top plan view of FIGURE 8.

DESCRIPTION OF THE PREFERRED EMBODIMENT:

Referring to FIGURE 1, one of skill in the art can ascertain that the lowest of the exploded parts of the figure is a base plate 10, which can be metallic or made of a conductive polymer such as a PTFE material partially plated with a conductive resin such as silver-epoxy resin composite. In the preferred embodiment, the metal used is copper but can be any conductive metal.

The base metal is coined to have a raised plateau area 30 of about 0.025 inch (0.64 mm) in thickness and a border region 20 of about 0.013 inch (0.33 mm) in thickness. The shape of the plateau area 30 is, as mentioned above, complimentary to the shape of the first dielectric frame layer 40. Most preferably, the raised plateau 30 of the base metal is in the shape of a square or rectangle when viewed from the top.

The preferred dielectric material comprises a filled fluoropolymeric material. Preferably the fluoropolymeric matrix comprises polytetrafluoroethylene (PTFE) with glass microfiber filler. The fluoropolymer matrix may also contain a suitable inorganic filler material such as ceramic powder (TiO_2, SiO_2 or alumina). Materials of this type are commonly available from Rogers Corporation of Rogers, Connecticut, under the trademark RT/Duroid with a more preferred material comprising glass microfiber reinforced PTFE sold under the trademark RT/Duroid 5870. The most preferred material however, is a variant of RT/Duroid 5870 called Ultralam GH where cladding is not applied to the dielectric material by the manufacturer of the material. Utilizing the most preferred material both reduces cost of purchase of the material and provides for a superior product. The superiority of Ultralam GH is due to the better bonding properties of the unclad material. This particular material was chosen because of its known desirable electrical properties such as low permittivity, low loss, microwave compatibility, high temperature capability and ease of fabrication. The thickness of the dielectric material used, in order to meet space constraints and design impedance values is as little as 250 μm for each frame layer. The thickness of the dielectric material can, however, be as large as 5 mm (5000 μm).

After the base metal 10 is coined to the desired shape and thickness, the dielectric material, first layer, is cut into a frame 40, by a programmed router or a punch and die set, the latter being preferred, to be of a complimentary shape to the plateau 30 on the base material. In the preferred embodiment, the dielectric material is square or rectangularly shaped n its uter perimeter 50 and is punched

out in like shape to form its inner perimeter 60. The inner perimeter 60 is dimensioned to receive the plateau 30 of the base 10. In the embodiment shown in FIGURE 1, the first PTFE frame layer 40 has outer perimetrical dimensions of 190 x 230 mils (4.826 x 5.842 mm), inner perimetrical dimensions of 110 x 150 mils (2.794 x 3.810 mm) and a thickness of 20 mils (508 μm).

A lead frame is then provided having an outer perimetrical frame portion 80, usually in the shape of a square or rectangle. From the outer portion 80, a predetermined number of leads 100 extend inwardly and terminate where the inner ends 110 thereof define a predetermined shape 120. The shape defined by the inner ends 110 of the leads 100 will be substantially similar to the shape of the plateau 30 on the base metal 10 and the shape of the inner perimeter 60 of the first frame layer of dielectric material. More specifically, the shape defined by the inner ends 110 of the leads 100 has the same dimensions as the inner perimeter 60 of the first dielectric frame layer. This allows for placing the lead frame flatly on top of the first dielectric frame layer 40 such that the leads extend from beyond the outer perimetrical dimension 50 of this frame layer to, exactly, the inner perimetrical dimension 60 thereof. The lead material can be any conductive material depending upon the desired application with respect to parameters such as impedance, etc. Most preferred by the present inventors is .005 inch (127 μm) thick copper, beryllium-copper alloy, iron-nickel-cobalt alloy or iron-nickel alloy (alloy 42). In the embodiment of FIGURE 1 the leads themselves, individually, are 15 x 5 mils (381 x 127 μm) with spacing between each lead being as small as 10 mils (254 μm). However, the desirable thickness range is from 100 to 250 μm. This thickness range is sufficient to allow the leads to retain their shape in handling and so that they can be formed for matched impedance connection to the board on which the package will be mounted. The length of the leads extending outside of the carrier is also important to the operation of the chip carrier. A minimum distance of .030 inch from the edge of the dielectric material 50 and 140 from which the lead emerges to its termination point 90 after bending is required. Therefore, one must

take into account the thickness of the base plate and the thickness of the first dielectric frame layer 40 along with the type of mounting to be used when determining the length of lead to be used.

Subsequently, a second frame layer 130 of dielectric material is placed upon the leads. The dimensions of the second frame layer 130, referring still to the embodiment in FIGURE 1, are 190 x 230 mils (4.826 x 5.842 mm) outside dimension and 140 x 180 mils (3.556 x 4.572 mm) inside dimension. It will be appreciated that the outside dimension of the second dielectric frame layer is identical to the first frame layer but the inside dimensions differ. A brief review of FIGURE 2 will reveal that this allows for the inner ends 110 of the leads to be exposed for later connection to a chip by beam lead welds or wire bonds. In most cases, the width of the exposed leads are .015 inch, however, the acceptable range is up to .030 inch.

Once all of the components above mentioned are prepared, they are permanently and durably assembled using a direct bonding process. A direct bonding process was chosen as the method of assembly since this process fuses the dielectric in the sheet composites to each other and to the metal used in the package. Fusing the dielectric creates a sufficiently strong bond for reliable use of the product. Moreover, the use of direct bonding eliminates the compromises attendant the use of adhesives. Adhesives raise costs of production to unacceptable levels and they can compromise the thermal and electrical properties of the package. To accomplish the direct bonding, a clamp and a rapid heating/rapid cooling process are used. The purpose of having the temperature change rapidly is to ensure good adhesion between the surfaces and uniform embedding of the leads in the dielectric layers, without producing a lateral flow of material thus distorting the frame and widening the wall. It was determined by the inventors hereof that a 150 psi (1 MPa) pressure, applied by a frictionless clamping force, a rapid rise in temperature to about 388° C, holding the temperature at that level for a period of about 10 to 25 minutes and then rapid cooling was sufficient to embed and seal the leads in the

dielectric material yet avoid deformation of the package. This operation is most preferably executed in an aluminum fixture (not shown) designed to maintain each of the component parts in register. There was significant concern, before positive testing of the bonding method, over whether sufficient material flow would be developed to completely seal and embed the leads and whether there would not also be lateral flow which would distort the frame and widen the wall. Unexpectedly, however, as set forth above, the parameters used did accomplish the required sealing/embedding of the leads and experiments done to ascertain the degree of sealing and embedment revealed that complete embedment and sealing were achieved without unacceptable distortion of the dielectric frame layers.

After bonding and excising of the lead frame, the final chip carrier package is shown generally at 132 in FIGURE 3. The above described method of producing the high RF and microwave chip carrier 132 provides a very cost effective and novel product where conductor losses and dielectric losses are both minimal, permittivity is low and conductor dielectric geometry can be designed for matched impedance without resorting to very small lead widths and thicknesses.

One of skill in the subject art will immediately appreciate that the method and basic design parameters of the invention described herein can be used to provide many different kinds and shapes of chip carriers; and by no means is the invention considered to be limited to the exact embodiments disclosed herein. The above description is only the most preferred embodiment and it must be understood that variations are within the scope of this invention.

One variation of significant importance is that the metal base plate 10 can be replaced by the dielectric material which is partially covered (in the area under the die which is the plateau region 30), with a conductive resin, preferably silver-epoxy resin composition. This can be done in the present invention or in prior art packages and can greatly reduce the cost of providing an adequate ground plane for the Gallium arsenide (GaAs) die.

It is also within the ambit of this disclosure to produce multi-layer packages and multi-die packages.

FIGURE 4 is a variation of the preferred embodiment. FIGURE 4 shows five Rf leads 100' and three DC leads 100"; other than this difference from the embodiment in FIGURE 1 the device is the same. A base plate, first dielectric layer, lead frame and second dielectric layer are all used to form the embodiment of FIGURE 4. The difference is that the leads are shaped differently for impedance matching. This is an example of one of the many alternative lead designs that can be provided.

FIGURE 5 depicts an alternative embodiment of the present invention, generally used in connection with direct broadcast satellites, where the raised plateau portion 30 of base metal 10 is smaller than the inner perimetrical dimension 60 of the first dielectric frame layer 40, whereby a gap 67 is formed between the two components in the region where they would normally engage. The gap formed is .005 inch wide and functions to provide flow space for the solder alloy (typically gold-tin eutectic), used to attach the die to the raised plateau, so it does not short circuit the leads.

FIGURE 6 depicts a further embodiment of the invention which is a replacement for a multichip type of chip carrier wherein the overall construction is elongated. Visible in the figure are base plate 10, first dielectric frame layer 40, leads 100 and second dielectric frame layer 130. It should be noted that in this embodiment, no raised plateau region (designated as 30 in other figures) has been provided. This benefits the particular utility of this carrier by allowing layers under the chips; that is, the package is used for a small circuit board already populated with several chips.

FIGURE 7 is a replacement for a conventional Dual-in-line package (DIP) which has been made by the method disclosed and claimed herein. Visible on the edge of FIGURE 7 are base plate 10, first dielectric frame layer 40 and second dielectric frame layer 130; leads are also depicted as 100. The embodiment in this

figure is additionally covered with a metal or dielectric cover layer 170. The chief benefit of such a layer is to protect the package contents from contamination or handling damage. FIGURES 7a, 7b and 7c are similarly numbered and show the different plan views of FIGURE 7.

FIGURE 8 depicts yet another embodiment of this invention with the primary difference being that the entire carrier has been placed inside of a separate cover for even greater weather resistance.

In FIGURE 8 a mounting plate 180 is shown in place of base plate 10. Mounting plate 180 laterally extends beyond the chip carrier frame to allow the carrier to be attached to a board with fasteners. The embodiment also includes a top cover 190. This embodiment is generally used for high power applications. FIGURES 8a, 8b and 8c show the various plan views of FIGURE 8.

While preferred embodiments have been shown and described, various modifications and substitutions may be made thereto without departing from the spirit and scope of the invention. Accordingly, it is to be understood that the present invention has been described by way of illustration and not limitation.

What is claimed is:

CLAIM 1. Method of making a high radio frequency or microwave chip carrier package comprising the steps of:

a) providing a base plate;

b) providing a first dielectric frame layer similar in shape and dimension to an outer perimetrical dimension of the base plate and having an open center portion;

c) placing said first dielectric frame layer upon the base plate;

d) providing a lead frame means, said lead frame including a plurality of leads arranged in a preselected pattern, said leads each having a first end and a second end, said first ends collectively terminating at an outer frame and said second ends terminating at and defining an inner space;

e) arranging said lead frame so that said second ends of said leads terminate proximally to the inner perimetrical dimension of the first dielectric layer and so that the leads are supported on said first dielectric frame layer;

f) providing a second dielectric frame layer having a shape corresponding to the first dielectric frame layer with an outside perimetrical dimension corresponding to the first dielectric frame layer and an inner perimetrical dimension, which is larger than the inner perimetrical dimension of the first dielectric frame layer;

g) stacking the second dielectric frame layer upon the above elements such that said second layer is in line with said first frame layer;

h) subjecting all of the aforesaid elements to pressure and elevated temperature in order to bond the base plate, first dielectric frame, lead frame and second dielectric frame;

i) separating the outer portion of the lead frame from the leads;

whereby a high radio frequency or microwave chip carrier is produced.

CLAIM 2. Method of claim 1 wherein step (h) further includes the step of:

maintaining a preselected temperature for a predetermined time period followed by rapid cooling.

CLAIM 3. Method as claimed in claim 1 wherein the base plate is metallic.

CLAIM 4. Method as claimed in claim 1 wherein the base plate is selected from the group consisting of copper, beryllium-copper alloy, brass, iron-nickel alloy, and iron-nickel-cobalt alloy.

CLAIM 5. Method as claimed in claim 1 wherein the base plate is a fluoroplymeric composite with a plating of a electrically conductive composite thereon.

CLAIM 6. Method as claimed in claim 1 wherein the dielectric material is a filled fluoropolymeric material.

CLAIM 7. Method as claimed in claim 5 wherein the dielectric material is Polytetrafluoroethylene.

CLAIM 8. Method as claimed in claim 5 wherein the PTFE is filled with an inorganic filler material.

CLAIM 9. Method as claimed in claim 6 wherein the inorganic filler material is ceramic powder.

CLAIM 10. Method as claimed in claim 7 wherein the ceramic powder is selected from the group consisting of SiO_2, TiO_2 and alumina.

CLAIM 11. Method as claimed in claim 6 wherein the filler material is glass microfiber.

CLAIM 12. Method as claimed in claim 6 wherein the filler material is glass microfiber and ceramic filler.

CLAIM 13. Method as claimed in claim 1 wherein the dielectric material is machined to a predetermined shape using a programmed router.

CLAIM 14. Method as claimed in claim 1 wherein the dielectric material is machined to a predetermined shape using a punch and die set.

CLAIM 15. A method as claimed in claim 1 wherein the lead frame material is selected from the group consisting of copper, beryllium-copper alloy, brass, iron-nickel alloy, and iron-nickel-cobalt alloy.

CLAIM 16. A method as claimed in claim 1 wherein the pressure exerted upon the component parts is by a frictionless clamping device.

CLAIM 17. Method as claimed in claim 16 wherein the pressure exerted is about 150 psi (1 MPa) of pressure.

CLAIM 18. Method as claimed in claim 2 wherein the rapidly rising temperature peaks at about 388° C and remains at that temperature for 10 to 25 minutes.

CLAIM 19. Method as claimed in claim 1 wherein step h includes a rapid heating of the elements.

CLAIM 20. Method of making a high radio frequency or microwave chip carrier package as claimed in claim 1 wherein the base plate also includes a raised plateau which engages with the opening in the first dielectric frame layer.

CLAIM 21. Method of making a high radio frequency or microwave chip carrier package as claimed in claim 1 wherein each layer is prefabricated as an array of one or more rows and columns joined by webs of the layer materials, to be subsequently severed after a single bonding step to produce many units from one bonding step.

CLAIM 22. A high frequency radio or microwave chip carrier package comprising:

a) a base plate;

b) a first dielectric frame layer similar in shape and dimension to an outer perimetrical dimension of the base plate and having an open center portion;

c) lead frame means having a plurality of leads arranged in a preselected pattern, said leads each having a first end and a second end, said first ends collectively terminating at an outer frame and said second ends terminating at and defining an inner space wherein the second ends terminate proximally to the inner primetrical dimension of the first dielectric frame layer and a portion of said leads proximal to the second ends thereof are supported by the first dielectric frame layer; and

d) a second dielectric frame layer with an outside perimetrical dimension corresponding to the first dielectric frame layer and an inner perimetrical dimension which is larger than the inner perimetrical dimension of the first dielectric frame layer;

whereafter all of the above elements are stacked in order of appearance and bonded using pressure and high temperature.

CLAIM 23. A high frequency radio or microwave chip carrier package as claimed in claim 22 wherein the base plate is metallic.

CLAIM 24. A high frequency radio or microwave chip carrier package as claimed in claim 22 wherein the base plate is selected from the group consisting of copper, beryllium-copper alloy, brass, iron-nickel alloy, and iron-nick-cobalt alloy.

CLAIM 25. A high frequency radio or microwave chip carrier package as claimed in claim 22 wherein the base plate is a fluoropolymeric composite with a plating of a electrically conductive composite thereon.

CLAIM 26. A high frequency radio or microwave chip carrier package as claimed in claim 22 wherein the dielectric material is a filled fluoropolymeric material.

CLAIM 27. A high frequency radio or microwave chip carrier package as claimed in claim 22 wherein the base plate is a fluoropolymeric composite with a plating of a electrically conductive composite thereon.

CLAIM 28. A high frequency radio or microwave chip carrier package as claimed in claim 22 wherein the PTFE is filled with an inorganic filler material.

CLAIM 29. A high frequency radio or microwave chip carrier package as claimed in claim 22 wherein the inorganic filler material is ceramic powder.

CLAIM 30. A high frequency radio or microwave chip carrier package as claimed in claim 22 wherein the ceramic powder is selected from the group consisting of $SI0_2$, $TI0_2$ and alumina.

CLAIM 31. A high frequency radio or microwave chip carrier package as claimed in claim 22 wherein the filler material is glass microfiber.

CLAIM 32. A high frequency radio or microwave chip carrier package as claimed in claim 22 wherein the filler material is glass microfiber and ceramic filler.

CLAIM 33. A high frequency radio or microwave chip carrier package as claimed in claim 22 wherein the dielectric material is machined to a predetermined shape using a programmed router.

CLAIM 34. A high frequency radio or microwave chip carrier package as claimed in claim 22 wherein the dielectric material is machined to a predetermined shape using a punch and die set.

CLAIM 35. A high frequency radio or microwave chip carrier package as claimed in claim 22 wherein the lead frame material is selected from the group consisting of copper, beryllium-copper alloy, brass, iron-nickel alloy, and iron-nickel-cobalt alloy.

CLAIM 36. A high frequency radio or microwave chip carrier package as claimed in claim 22 wherein the pressure exerted upon the component parts is by a frictionless clamping device.

CLAIM 37. A high frequency radio or microwave chip carrier package as claimed in claim 22 wherein the pressure exerted is about 150 psi (1 MPa) of pressure.

CLAIM 38. A high frequency radio or microwave chip carrier package as claimed in claim 22 wherein the base plate also includes a raised plateau which engages with the opening in the first dielectric frame layer.

CLAIM 39. A high frequency radio or microwave chip carrier package as claimed in claim 22 wherein each layer is prefabricated as an array of one or more rows and columns joined by webs of the layer materials, to be subsequently severed after a single bonding step to form many units from one bonding step.

CLAIM 40. A bonded chip carrier package for high frequency radio and microwave applications produced by a process including the steps of:

a) providing a base plate;

b) providing a first dielectric frame layer similar in shape and dimension to an outer perimetrical dimension of the base plate and having an open center portion;

c) placing said first dielectric frame layer upon the base plate;

d) providing a lead frame means, said lead frame including a plurality of leads arranged in a preselected pattern, said leads each having a first end and a second end, said first ends collectively terminating at an outer frame and said second ends terminating at and defining an inner space;

e) arranging said lead frame so that said second ends of said leads terminate proximally to the inner perimetrical dimension of the first dielectric layer and so that the leads are supported on said first dielectric frame layer;

f) providing a second dielectric frame layer having a shape corresponding to the first dielectric frame layer with an outside perimetrical dimension corresponding to the first dielectric frame layer and an inner perimetrical dimension, which is larger than the inner perimetrical dimension of the first dielectric frame layer;

g) stacking the second dielectric frame layer upon the above elements such that said second layer is in line with said first frame layer;

h) subjecting all of the aforesaid elements to pressure and elevated temperature in order to bond the base plate, first dielectric frame, lead frame and second dielectric frame;

i) separating the outer portion of the lead frame from the leads;

whereby a high radio frequency or microwave chip carrier is produced.

CLAIM 41. Method of making a high radio frequency or microwave chip carrier package comprising the steps of:

a) providing a first dielectric frame layer;

b) providing a lead frame means, said lead frame including a plurality of leads arranged in a preselected pattern, said leads each having a first end and a second end, said first ends collectively terminating at an outer frame and said second ends terminating at and defining an inner space;

c) arranging said lead frame so that said second ends of said leads terminate concentrically with an axis of said first dielectric layer and so that the leads are supported on said first dielectric frame layer;

d) providing a second dielectric frame layer having a shape corresponding to the first dielectric frame layer with an outside perimetrical dimension corresponding to the first dielectric frame layer and an inner perimetrical dimension, which is larger than the perimetrical dimension defined by the second ends of the leads;

e) stacking the second dielectric frame layer upon the above elements such that said second layer is in line with said first frame layer;

f) subjecting all of the aforesaid elements to pressure and elevated temperature in order to bond the first dielectric frame, lead frame and second dielectric frame;

g) separating the outer portion of the lead frame from the leads;

whereby a high radio frequency or microwave chip carrier is produced.

CLAIM 42. A high frequency radio or microwave chip carrier package comprising:

a) a first dielectric frame layer;

b) lead frame means having a plurality of leads arranged in a preselected pattern, said leads each having a first end and a second end, said first ends collectively terminating at an outer frame and said second ends terminating concentrically with the first dielectric frame layer and a portion of said leads proximal to the second ends thereof are supported by the first dielectric frame layer; and

c) a second dielectric frame layer with an outside perimetrical dimension corresponding to the first dielectric frame layer and an inner perimetrical dimension which is larger than the space defined by the second end of the leads;

whereafter all of the above elements are stacked in order of appearance and bonded using pressure and high temperature.

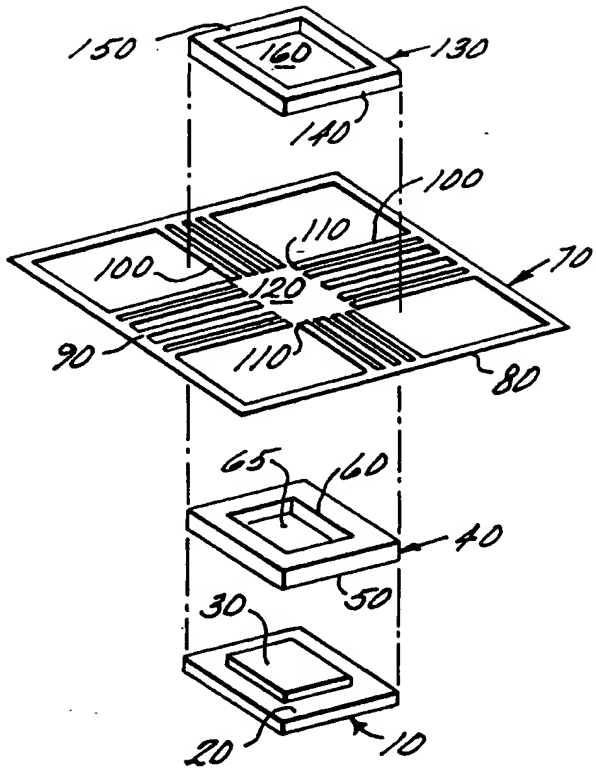

FIG. 1

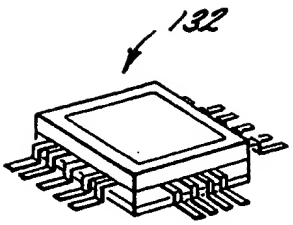

FIG. 3

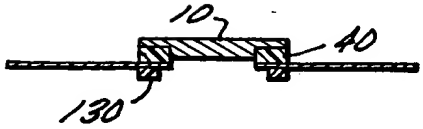

FIG. 2b

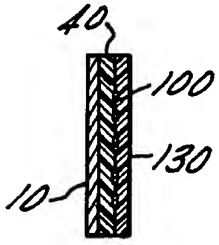

FIG. 2a

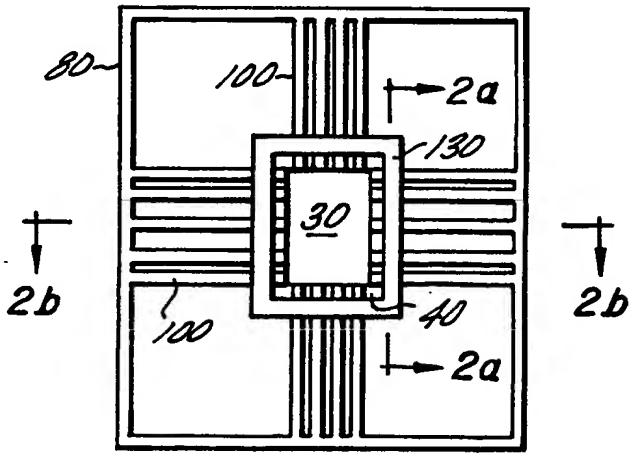

FIG. 2

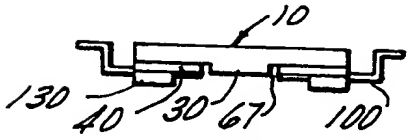

FIG. 5a

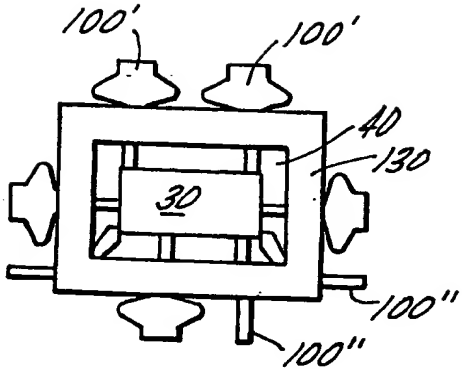

FIG. 4

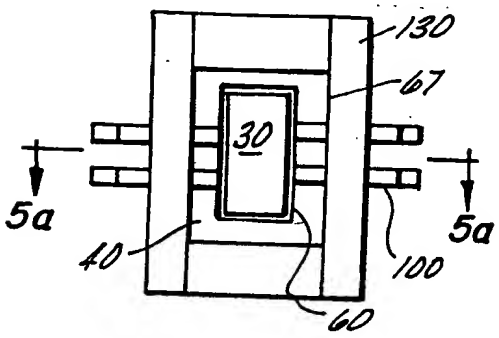

FIG. 5

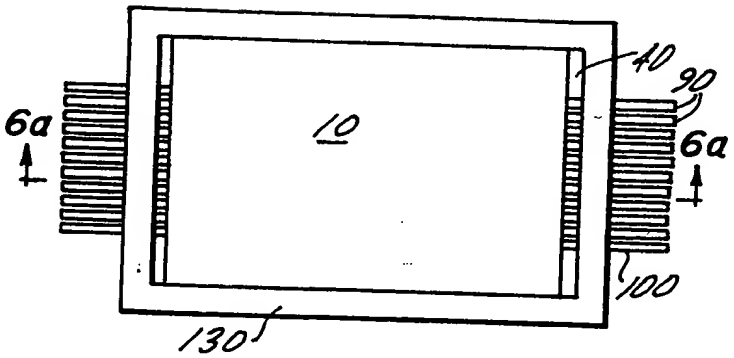

FIG. 6

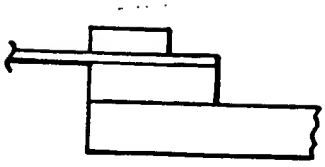

FIG. 6b

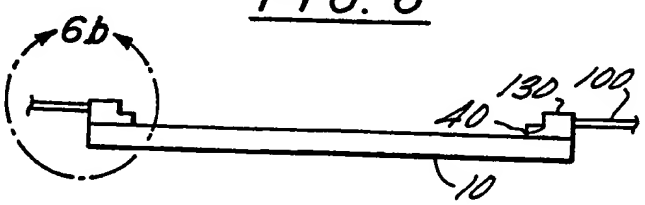

FIG. 6a

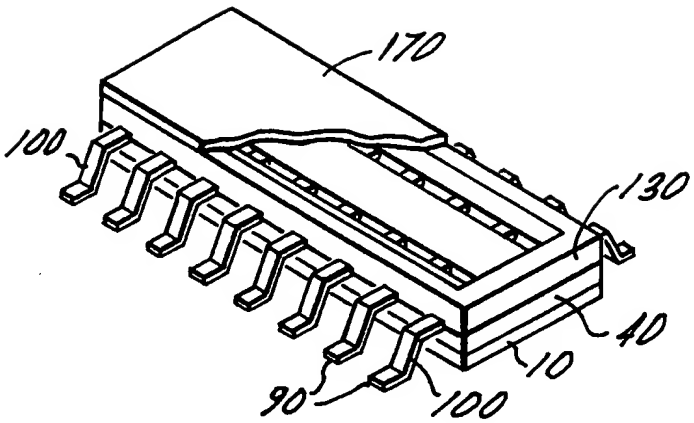

FIG. 7

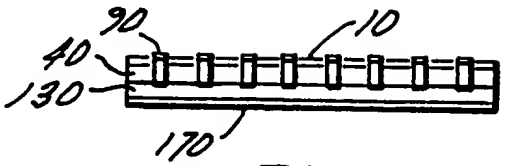

FIG. 7a

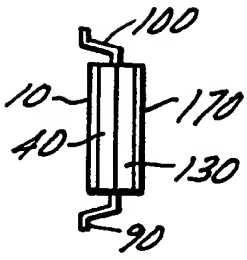

FIG. 7b

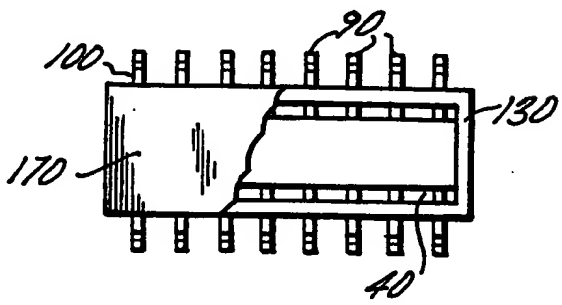

FIG. 7c

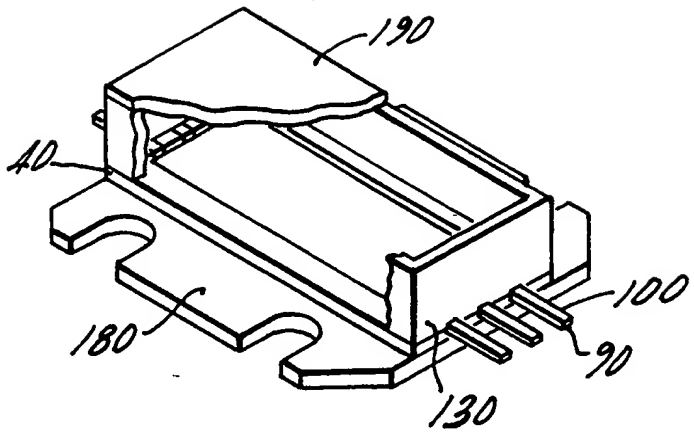

FIG. 8

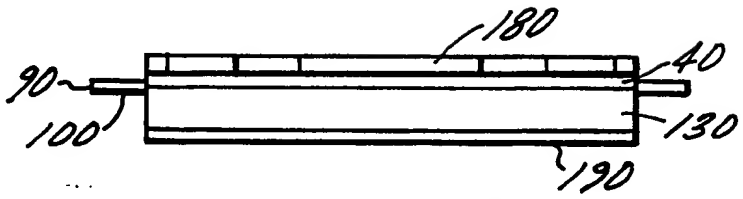

FIG. 8a

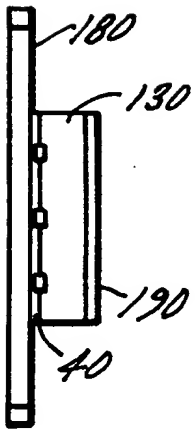

FIG. 8b

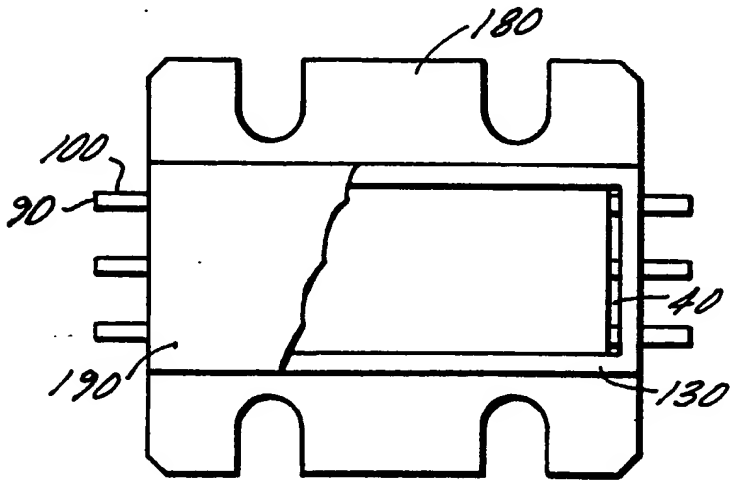

FIG. 8c

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/12460

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 23/02
US CL :174/52.4;257/728,795
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 174/51.1-52.4;257/678,688,692,700-703,711,728,729,746,795;361/723

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US,A, 5,159,432(OHKUBO ET AL) 27 October 1992, see entire document.	1-42
Y,P	US,A, 5,331,511 (LEE ET AL) 19 July 1994, see Figure 3.	1-42
A,E	US,A, 5,381,037(OLIVAREZ) 10 January 1995, see entire document.	1-42
A	US,A, 5,225,709 (NISHIUMA ET AL) 06 July 1993, entire document.	1-42
A	US,A, 5,258,575 (BEPPU ET AL) 02 November 1993, see entire document.	1-42

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
10 MARCH 1995	29 MAR 1995
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer CHRIS HORGAN Telephone No. (703) 308-3748

Form PCT/ISA/210 (second sheet)(July 1992)*